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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,948	11/20/2001	Kun-Lin Wu	UMC-98-254 CON2	4310

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EXAMINER	
YEVSIKOV, VICTOR V	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,948	WU ET AL.	
	Examiner	Art Unit	
	Victor V Yevsikov	2825	

-- Th MAILING DATE of this communication app ars n th cov r sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-31 and 33-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-31 and 33-64* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/132,876.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 32 objected to because of the following informalities: claim 32 is a copy of claim 31. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 28, 30, 31, 33, 34, 36-38, 41, 42, 44, 45, 47-51, 53-55, 57-61, 63 and 64 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 6,008,120).

With respect to claims 28, 30, 31, 33, 34, 36-38, 41, 42 and 44 Lee teaches a chemical-mechanical polishing process, comprising the steps of:

forming a first conductive layer 22 and a dielectric layer 23, 24, and 25 over a semiconductor substrate;

polishing the dielectric layer 24, 25 to form a substantially planar surface 24b, 25b; forming a dielectric cap layer 26 over the dielectric layer, and wherein:

the step of forming the dielectric layer includes a high-density plasma chemical vapor deposition method;

the step of forming the dielectric layer includes depositing silicon dioxide;

the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition method with silane (SiH4) as the main reactive agent;

the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules;

the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules;

the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silane (SiH4) as the main reactive agent;

the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules;

the step of forming the cap layer includes depositing silicon dioxide;

the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

Reference: Figs. 1A-1C, 2A-2C with corresponding text.

With respect to claims 45, 47-51 and 53-54 Lee teaches a chemical mechanical polishing process,

comprising the steps of:

forming a conductive layer 22 over a semiconductor substrate;

patterning the conductive layer 22 to form interconnect lines;

forming at least one dielectric layer 23,24,25 over the interconnect lines, the at least one dielectric layer 24 having a first thickness;

polishing the at least one dielectric layer to form a planar surface 24b,25b;

forming a thin cap layer 26 over the planar surface, the thin cap layer having a second thickness which is sufficient to fill scratches formed in the at least one dielectric layer during the polishing step, and which second thickness is substantially less than the first thickness (figs. 1B, 1C), and wherein:

the first thickness is about ten times greater than the second thickness;

the cap layer prevents metal bridges from forming in the scratches of the at least one dielectric layer;

the at least one dielectric layer includes a fluorinated silicon glass (FSG) layer;

the at least one dielectric layer further includes a high density plasma chemical vapor deposition layer formed between and over the interconnect lines;

the cap layer includes silicon oxide, silicon nitride, phosphosilicate glass (PSG), and/or silicon-rich oxide;

the cap layer provides a higher degree of surface planarity than the planar surface, and further forms a highly planar surface that can reduce undesirable diffractions from height differences so that during a subsequent photolithographic operation undesirable diffractions from height differences are reduced;

the further including the steps of:

patterning the cap layer 44 and the at least one dielectric layer to form openings to the conductive layer 47;

forming an additional conductive layer 47 over the cap layer and in the openings, such that conductive vias are formed between the conductive layer and the additional conductive layer;

patterning the additional conductive layer to form additional interconnects over the cap layer. (fig. 3; col.11, lines 35-58).

Reference: figs. 1A-3 with corresponding text.

With respect to claims 55, 57-61, 63 and 64 Lee teaches a chemical mechanical polishing process, comprising the steps of:

forming a conductive layer over a semiconductor substrate;

patterning the conductive layer to form interconnect lines;

forming at least one dielectric layer over the interconnect lines, the at least one dielectric layer having a first thickness;

polishing the at least one dielectric layer to form a polished surface; and

forming a thin cap layer over the polished surface to planarize the polished surface, the thin cap layer having a second thickness which is substantially less than the first thickness and wherein:

the first thickness is about ten times greater than the second thickness.

the cap layer prevents metal bridges from forming in the scratches of the at least one dielectric layer.

the at least one dielectric layer includes a fluorinated silicon glass (FSG) layer.

the at least one dielectric layer further includes a high density plasma chemical vapor deposition layer formed between and over the interconnect lines.

the cap layer includes silicon oxide, silicon nitride, phosphosilicate glass (PSG), and/or silicon-rich oxide.

the cap layer provides a higher degree of surface planarity than the planar surface, and further forms a highly planar surface that can reduce undesirable diffractions from height differences so that during a subsequent photolithographic operation undesirable diffractions from height differences are reduced.

the further including the steps of:

patterning the cap layer and the at least one dielectric layer to form openings to the conductive layer;

forming an additional conductive layer over the cap layer and in the openings, such that conductive vias are formed between the conductive layer and the additional conductive layer;

patterning the additional conductive layer to form additional interconnects over the cap layer.

Reference: figs. 1A-3 with corresponding text.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29, 52 and 62 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Jain (US 5,494,854).

Lee discloses the features out lined above, but does not show exactly a method wherein the step of forming the conductive layer includes depositing doped polysilicon.

However, Jain teaches the method wherein the step of forming the conductive layer includes depositing doped polysilicon (Table.2).

It would have been obvious to those skilled in the art using the polysilicon for forming conductive layer as taught by Lee/Jain for provides process as is routine in the art.

Claims 35, 39 and 43 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Jain (US 5,494,854).

Lee discloses the features out lined above, but does not show exactly a method wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition method with tetra-ethyl-ortho-silicate (TEOS) or silicon dichlorohydride (SiH_2C1_2) or silicon rich oxide (SRO) as the main reactive agent.

However, Jain teaches the method wherein the step of depositing a silicon oxide layer using a chemical vapor deposition method with tetra-ethyl-ortho-silicate (TEOS) or silicon dichlorohydride (SiH_2C1_2) or silicon rich oxide (SRO) as the main reactive agent (col.2, lines 28-62).

It would have been obvious to those skilled in the art using the TEOS or (SiH_2C1_2) or SRO for forming silicon oxide cap layer as taught by Lee/Jain for provides process as is routine in the art.

Claims 40, 46 and 56 are rejected as being prima facie obvious without showing that the claimed ranges (concentration, thickness, temperature, process time) achieve unexpected results relative to the prior art range.

In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (703) 3050758. The examiner can normally be reached by telephone on Monday to Friday 7:15 AM to 4:45 PM (except second Mondays).

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or processing is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7033080596.

Victor Yevsikov

December 18, 2003